REMARKS

I. General

Claims 1-53 are pending, and all are rejected by the Office Action mailed December 29, 2004. No claims are amended by this response. The issues in the current Office Action are as follows:

- Claims 1-9, 11-18, 25, 26, 35, 36, 43, and 44 are rejected under 35 U.S.C. §102(b) as being anticipated by US Patent 5,463,620 (hereinafter, *Sriram*).
- Claims 10, 19-24, and 37-42 are rejected under 35 U.S.C. §103(a) as being obvious over *Sriram*.
- Claims 27-34, and 45-53 are rejected under 35 U.S.C. §103(a) as being obvious over *Sriram* in view of Sally Floyd and Van Jacobson, Random Early Detection Gateways for Congestion Avoidance, August 1993, IEEE/ACM Transactions on Networking (hereinafter, *RED*).

Applicant hereby traverses the rejections and requests reconsideration and withdrawal in light of the remarks contained herein.

II. Rejections Under 35 U.S.C. §102(b)

Claims 1-9, 11-18, 25, 26, 35, 36, 43, and 44 are rejected under 35 U.S.C. §102(b) as being anticipated by *Sriram*. Applicant traverses the rejections.

A. Claims 1-9

To anticipate a claim under 35 U.S.C. § 102, a reference must teach every element of the claim, see M.P.E.P. § 2131. Moreover, in order for an applied reference to be anticipatory under 35 U.S.C. § 102 with respect to a claim, "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim," see M.P.E.P. § 2131, citing *Richardson v. Suzuki Motor Co.*, 9 U.S.P.Q.2d 1913 (Fed. Cir. 1989). As discussed further below, these requirements are not satisfied by the 35 U.S.C. § 102 rejection because *Sriram* does not teach every element of the claims.

Claim 1 recites, in part, "a common shared memory device interconnected with all of said plurality of queues." *Sriram* does not teach at least this feature of claim 1. The Office Action states at page 3:

> [I]t is inherent that each of the parallel queues 1 through n in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45[.]

The current rejection is incorrect for two reasons. First, the concept of inherency has not been applied correctly. The rejection merely asserts that the above-recited feature of claim 1 is inherent because the output queues of *Sriram* "*can* all be located on a shared memory device." (emphasis added). However, inherency requires that the missing feature be "necessarily present in the thing described in the reference." *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991). Therefore, it is not enough under the law to assert that a missing feature can be present in the applied reference, rather, the law requires that the missing feature must be present, although not explicitly described. The current rejection fails to meet the standard set by law because it does not assert that the output queues of *Sriram* are necessarily all located on a shared memory device. Further, the Examiner must "provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." See M.P.E.P. §2112(IV), citing *Ex Parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat App. & Inter. 1990). In other words, it is not enough to allege that a limitation is present in a reference—there must be reasoning that shows that the limitation must be in the reference. The Office Action, however, merely asserts that the claimed limitation is inherent and does not give reasoning or evidence tending to show that such feature is necessarily present in *Sriram*.

It should also be noted that the assertion of inherency is unclear. The Office Action states, "[I]t is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device..." Office Action at 3. It appears that the Office Action asserts that the queues in figure 5, in addition to the queues in figure 6, can all be located on the same memory device. However, the queues in figure 5 are the same queues that are depicted in figure 6. (Notice how all queues output to item 28 in both figures 5 and 6.) It makes no

sense to say that queues are located on the same memory device with themselves. Further, if the Office Action intends to state that *Aatresh* teaches two sets of queues on one memory device, such assertion is incorrect, as *Aatresh* shows one set of output queues on the DRAM buffer of figure 4. Accordingly, Applicant requests a reference that teaches what is asserted by Official Notice, as provided by M.P.E.P. §2144.03(C). Accordingly, no prima facie case of anticipation is made.

Second, the reference does not teach the above-recited feature at least because it does not describe the memory device or devices used in the queues of *Sriram*. One of skill in the art might assume that each queue uses its own memory device, and such an assumption would not be inconsistent with the teaching of the cited passages of *Sriram*, which do not teach use of any particular memory structures. Thus, merely teaching queues with nothing more is not enough to teach, "a common shared memory device interconnected with all of said plurality of queues," as in claim 1. Accordingly, *Sriram* does not teach the above-recited feature of claim 1.

Further, claim 1 recites, in part, "a queue congestion processor interconnected with said input terminals of all of said queues." *Sriram* does not teach at least this feature of claim 1. The Office Action cites the ATM switch fabric of figure 3 and the passage at column 4, lines 59-63. However, such assertion is incorrect. While *Sriram* does teach allocating bandwidth to multiple calls in such passages as column 3, lines 43-55, column 5, line 51 through column 6, line 62, and column 10, lines 1-16, it does not actually address the issue of queue congestion. The table lookups cited by the Office Action do not address queue congestion, but rather, only indicate the amount of bandwidth that should be allocated to each call type. See Col. 7, lines 25-55. The amount of bandwidth that should ideally be available for a call is not enough, by itself, to teach queue congestion. Accordingly, *Sriram* does not teach, "a queue congestion processor interconnected with said input terminals of all of said queues," as recited by claim 1.

Dependent claims 2-9 each depend either directly or indirectly from independent claim 1 and, thus, inherit all of the limitations of independent claim 1. Thus, *Sriram* does not teach all claim limitations of claims 2-9. It is respectfully submitted that dependent claims 2-9 are allowable at least because of their dependence from claim 1 for the reasons discussed

above. Therefore, it is respectfully requested that the rejection of claims 1-9 be withdrawn and those claims allowed.

B. Claims 11-18, 25, and 26

Claim 11 recites, in part, "storing said packet payloads in a common memory pool shared by all of said plurality of queues." *Sriram* does not teach at least this feature of claim 11.

The Office Action states at page 5:

> [I]t is inherent that each of the parallel queues 1 through n in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45[.]

The current rejection is incorrect for two reasons. First, the concept of inherency has not been applied correctly. The rejection merely asserts that the above-recited feature of claim 11 is inherent because the output queues of *Sriram* "*can* all be located on a shared memory device." (emphasis added). However, inherency requires that the missing feature be "necessarily present in the thing described in the reference." *Continental Can*, 20 U.S.P.Q.2d 1746, 1749. Therefore, it is not enough under the law to assert that a missing feature can be present in the applied reference, rather, the law requires that the missing feature must be present, although not explicitly described. The current rejection fails to meet the standard set by law because it does not assert that the output queues of *Sriram* are necessarily all stored in a common memory pool. Further, the Examiner must "provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." See M.P.E.P. §2112(IV), citing *Ex Parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat App. & Inter. 1990). In other words, it is not enough to allege that a limitation is present in a reference—there must be reasoning that shows that the limitation must be in the reference. The Office Action, however, merely asserts that the claimed limitation is inherent and does not give reasoning or evidence tending to show that such feature is necessarily present in *Sriram*. Further, Official Notice does not assert that a common memory pool is taught, only that a shared memory device is taught. It should be noted that a shared memory device is not necessarily the same as a common memory pool. For instance, a memory device may be partitioned such that each

part is used by a different queue, thereby utilizing a shared memory device, but not a common memory pool. Accordingly, no prima facie case of anticipation is made.

It should also be noted that the assertion of inherency is unclear. The Office Action states, "[I]t is inherent that each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device..." Office Action at 5. It appears that the Office Action asserts that the queues in figure 5, in addition to the queues in figure 6, can all be located on the same memory device. However, the queues in figure 5 are the same queues that are depicted in figure 6. (Notice how all queues output to item 28 in both figures 5 and 6.) It makes no sense to say that queues are located on the same memory device with themselves. Further, if the Office Action intends to state that *Aatresh* teaches two sets of queues on one memory device, such assertion is incorrect, as *Aatresh* shows one set of output queues on the DRAM buffer of figure 4. Accordingly, Applicant requests a reference that teaches what is asserted by Official Notice, as provided by M.P.E.P. §2144.03(C). Accordingly, no prima facie case of anticipation is made.

Second, the reference does not teach the above-recited feature at least because it does not describe the memory device or devices used in the queues of *Sriram*. One of skill in the art might assume that each queue uses its own memory pool, and such an assumption would not be inconsistent with the teaching of the cited passages of *Sriram*, which do not teach use of any particular memory structures. Thus, merely teaching queues with nothing more is not enough to teach, "storing said packet payloads in a common memory pool shared by all of said plurality of queues," as in claim 11. Accordingly, *Sriram* does not teach the above-recited feature of claim 11.

Additionally, claim 11 recites, in part, "storing said packet payload pointers in said queues." *Sriram* does not teach at least this feature of claim 11.

The Office Action states at page 5:

> [E]xaminer also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, inherently one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44[.]

The current rejection is incorrect for two reasons. First, the concept of inherency has not been applied correctly. The rejection merely asserts that the above-recited feature of claim 11 is inherent because it "*can* be used in a router." (emphasis added). However, inherency requires that the missing feature be "necessarily present in the thing described in the reference." *Continental Can*, 20 U.S.P.Q.2d 1746, 1749. Therefore, it is not enough under the law to assert that a missing feature can be present in the applied reference, rather, the law requires that the missing feature must be present, although not explicitly described. The current rejection fails to meet the standard set by law because it does not assert that the recited features are necessarily present in *Sriram*. Further, the Examiner must "provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." See M.P.E.P. §2112(IV), citing *Ex Parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat App. & Inter. 1990). In other words, it is not enough to allege that a limitation is present in a reference—there must be reasoning that shows that the limitation must be in the reference. The Office Action, however, merely asserts that the claimed limitation is inherent and does not give reasoning or evidence tending to show that such feature is necessarily present in *Sriram*. Accordingly, no prima facie case of anticipation is made.

Second, *Sriram* simply does not teach the above-recited feature at least because it does not teach, "storing said packet payload pointers in said queues," as in claim 11. Accordingly, *Sriram* does not teach the above-recited feature of claim 11.

Dependent claims 12-18, 25, and 26 each depend either directly or indirectly from independent claim 11 and, thus, inherit all of the limitations of independent claim 11. Thus, *Sriram* does not teach all claim limitations of claims 12-18, 25, and 26. It is respectfully submitted that dependent claims 12-18, 25, and 26 are allowable at least because of their dependence from claim 11 for the reasons discussed above. Therefore, it is respectfully requested that the rejection of claims 11-18, 25, and 26 be withdrawn and those claims allowed.

C. Claims 35, 36, 43, and 44

Claim 35 recites, in part, "sharing a common memory pool." *Sriram* does not teach at least this feature of claim 35. The Office Action states at page 6:

> [I]t is inherent that each of the parallel queues 1 through n in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45[.]

The current rejection is incorrect for two reasons. First, the concept of inherency has not been applied correctly. The rejection merely asserts that the above-recited feature of claim 35 is inherent because the output queues of *Sriram* "*can* all be located on a shared memory device." (emphasis added). However, inherency requires that the missing feature be "necessarily present in the thing described in the reference." *Continental Can*, 20 U.S.P.Q.2d 1746, 1749. Therefore, it is not enough under the law to assert that a missing feature can be present in the applied reference, rather, the law requires that the missing feature must be present, although not explicitly described. The current rejection fails to meet the standard set by law because it does not assert that the output queues of *Sriram* are necessarily sharing a common memory pool. Further, the Examiner must "provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." See M.P.E.P. §2112(IV), citing Ex Parte Levy, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat App. & Inter. 1990). In other words, it is not enough to allege that a limitation is present in a reference—there must be reasoning that shows that the limitation must be in the reference. The Office Action, however, merely asserts that the claimed limitation is inherent and does not give reasoning or evidence tending to show that such feature is necessarily present in *Sriram*. Further, Official Notice does not assert that a common memory pool is taught, only that a shared memory device is taught. It should be noted that a shared memory device is not necessarily the same as a common memory pool. For instance, a memory device may be partitioned such that each part is used by a different queue, thereby utilizing a shared memory device, but not a common memory pool. Accordingly, no prima facie case of anticipation is made.

Second, the reference does not teach the above-recited feature of clam 35 at least because it does not describe the memory device or devices used in the queues of *Sriram*. One of skill in the art might assume that each queue uses its own memory pool, and such an assumption would not be inconsistent with the teaching of the cited passages of *Sriram*, which do not teach use of any particular memory structures. Thus, merely teaching queues with nothing more is not enough to teach, "sharing a common memory pool," as in claim 35. Accordingly, *Sriram* does not teach the above-recited feature of claim 35.

Additionally, claim 35 recites, in part, "A method of instantaneous queue congestion management of drop probabilities of packets." *Sriram* does not teach at least this feature of claim 35 because it does not teach drop probabilities. The Office Action cites the table lookup of traffic tables in *Sriram* at column 7, lines 30-36 as teaching the feature; however, such assertion is incorrect. The tables in the cited passage only indicate the bandwidth needed to multiplex calls of a particular subclass. In other words, the tables indicate an assumed ideal amount of bandwidth needed to pass given calls. *Sriram* does not teach any action with regard to drop probabilities; in fact, drop probabilities are not taught or mentioned by *Sriram*. Accordingly, this feature is not taught by *Sriram*.

Still further, claim 35 recites, in part, "using a queue congestion management algorithm." *Sriram* does not teach this feature. The Office Action cites the passage in *Sriram* at column 6, lines 57-62. The cited passage teaches time slice allocations, which is not the same as queue congestion management. The bandwidth allocation cited by the Office Action does not address queue congestion, but rather, only indicates the amount of bandwidth allocated to each call type as classes and sub-classes of call types change. While *Sriram* teaches allocating bandwidth to multiple calls in such other passages as column 3, lines 43-55, column 5, line 51 through column 6, line 62, and column 10, lines 1-16, it does not actually address the issue of queue congestion. Bandwidth allocation between call types is not enough, by itself, to teach queue congestion. Accordingly, *Sriram* does not teach, "using a queue congestion management algorithm," as recited by claim 35.

Dependent claims 36, 43, and 44 each depend either directly or indirectly from independent claim 35 and, thus, inherit all of the limitations of independent claim 35. Thus, *Sriram* does not teach all claim limitations of claims 36, 43, and 44. It is respectfully submitted that dependent claims 36, 43, and 44 are allowable at least because of their dependence from claim 35 for the reasons discussed above. Therefore, it is respectfully requested that the rejection of claims 35, 36, 43, and 44 be withdrawn and those claims allowed.

III. Rejections under 35 U.S.C. §103(a)

A. Rejections over Sriram

Claims 10, 19-24, and 37-42 are rejected under 35 U.S.C. §103(a) as being obvious over *Sriram*. Applicant traverses the rejection.

To establish a prima facie case of obviousness under 35 U.S.C. § 103(a), three basic criteria must be met. First, there must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the applied reference. Second, there must be a reasonable expectation of success. Finally, the applied reference must teach or suggest all the claim limitations. *See* M.P.E.P. § 2143. Without conceding any other criteria, Applicant respectfully asserts that the rejection does not satisfy the third criterion, as discussed further below.

Dependent claims 10, 19-24, and 37-42 each depend either directly or indirectly from respective independent claims 1, 11, and 35 and, thus, inherit all of the limitations of their respective independent claims. As shown above, *Sriram* does not teach each and every feature of claims 1, 11, and 35. The Office Action does not rely on other sources to teach or suggest those features that are shown to be missing in *Sriram*. Thus, *Sriram* does not teach or suggest all claim limitations of claims 10, 19-24, and 37-42. It is respectfully submitted that dependent claims 10, 19-24, and 37-42 are allowable at least because of their dependence from claims 1, 11, and 35 for the reasons discussed above. Therefore, it is respectfully requested that the rejection of claims 10, 19-24, and 37-42 be withdrawn and those claims allowed.

B. Rejections over Sriram in view of RED

Claims 27-34, and 45-53 are rejected under 35 U.S.C. §103(a) as being obvious over *Sriram* in view of *RED*. Applicant traverses the rejection.

1. Claims 27-34

a. Failure to teach or suggest all claim limitations

Dependent claims 27-34 each depend either directly or indirectly from independent claim 11 and, thus, inherit all of the limitations of independent claim 11. As shown above,

Sriram does not teach each and every feature of claim 11. The Office Action does not rely on *RED* or any other reference to teach or suggest those features that are shown to be missing in *Sriram*. Thus, the cited combination does not teach or suggest all claim limitations of claims 27-34. It is respectfully submitted that dependent claims 27-34 are allowable at least because of their dependence from claim 11 for the reasons discussed above. Therefore, it is respectfully requested that the rejection of claims 27-34 be withdrawn and those claims allowed.

b. Lack of motivation to combine references

The Office Action states, with regard to claim 27:

> [I]t is obvious, and therefore, examiner takes Official Notice that each of the parallel queues 1 through n in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, inherently one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44.

Office Action at 15. The Office Action further states, with regard to claim 28:

> Examiner takes Official Notice that it is obvious to implement an algorithm in hardware. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the algorithm in either software or hardware.

Office Action at 16. As shown above in the quoted sections, the Office Action states that 1) it is obvious to employ a shared memory device, 2) it is obvious to implement one of many memory structures that can be used in a router, and 3) it is obvious to implement an algorithm in hardware. The Office Action, however, fails to suggest the desirability for any of the suggested modifications. It is well settled that the fact that references can be combined or modified is not sufficient to establish a *prima facie* case of obviousness, M.P.E.P. § 2143.01. The quoted statements above merely say that the references can be modified, and do not state any desirability for making the modifications. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combinations, M.P.E.P. § 2143.01 citing *In re Mills*, 16

U.S.P.Q.2d 1430 (Fed. Cir. 1990). Thus, the failure to provide motivation suggesting desirability of the modifications is improper. Accordingly, Applicant respectfully submits that the 35 U.S.C. § 103(a) rejection of claims 27 and 28 are improper and should be withdrawn.

2. Claims 45-53

a. Failure to teach or suggest all claim limitations

Additionally, claim 45 recites, in part, "A method of time-averaged congestion management of drop probabilities of packets." The combination does not teach at least this feature of claim 45 because it does not teach drop probabilities. The Office Action states:

> [W]hen performing statistical multiplexing, the queues are checked for actual size in order to determine whether to admit a call depending on the class of call and the already-partitioned bandwidth allocated (i.e., how many QOS-specific queues are already filled), col. 2, lines 21-23, if the packet is not admitted, it is 'dropped[.]'

Office Action at 19. The Office Action's assertions are incorrect. First, the cited passages say nothing about checking queues for actual size nor do they mention or teach queue congestion. Second, the determination to deny a call does not result in packets being dropped, it simply results in the originating switch trying alternate routes to complete the call. See Col. 10, lines 9-12. Third, the cited passage (column 2, lines 21-23) only teaches that multiple calls are multiplexed into a single queuing circuit. The cited passage does not teach or suggest any action with regard to drop probabilities; in fact, drop probabilities are not taught or mentioned by *Sriram*. Accordingly, this feature is not taught or suggested by *Sriram*. The Office Action does not rely on *RED* to teach or suggest the feature; therefore, the cited combination does not teach or suggest this feature.

Further, claim 45 recites, in part, "applied to a plurality of arrays sharing a common memory pool." The Office Action takes Official Notice that the output queues of *Sriram* "can all be located on a shared memory device," and asserts that the feature is taught by such a system. However, the Official Notice does not assert that sharing a common memory pool is taught or suggested, only that a shared memory device is taught or suggested. It should be noted that a shared memory device is not necessarily the same as a common memory pool. For instance, a memory device may be partitioned such that each part is used by a different

queue, thereby utilizing a shared memory device, but not a common memory pool. Accordingly, even with Official Notice, the combination does not teach or suggest each and every feature.

It should be noted, however, that Official Notice is used to show that " each of the parallel queues 1 through *n* in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device..." Office Action at 19. It appears that the Office Action asserts that the queues in figure 5, in addition to the queues in figure 6, can all be located on the same memory device. However, the queues in figure 5 are the same queues that are depicted in figure 6. (Notice how all queues output to item 28 in both figures 5 and 6.) It makes no sense to say that queues are located on the same memory device with themselves. Further, if the Office Action intends to state that *Aatresh* teaches two sets of queues on one memory device, such assertion is incorrect, as *Aatresh* shows one set of output queues on the DRAM buffer of figure 4. Accordingly, Applicant requests a reference that teaches what is asserted by Official Notice, as provided by M.P.E.P. §2144.03(C). Still, further, the language of the rejection asserts that "the pointer-payload memory and queuing structure" is "well-known in the art;" however, the claim does not specify a pointer-payload memory and queuing structure, and, therefore, such statement is irrelevant to claim 45.

Dependent claims 46-53 each depend either directly or indirectly from independent claim 45 and, thus, inherit all of the limitations of independent claim 45. As shown above, *Sriram* does not teach each and every feature of claim 45. The Office Action does not rely on *RED* or any other reference to teach or suggest those features that are shown to be missing in *Sriram*. Thus, the cited combination does not teach or suggest all claim limitations of claims 46-53. It is respectfully submitted that dependent claims 46-53 are allowable at least because of their dependence from claim 45 for the reasons discussed above. Therefore, it is respectfully requested that the rejection of claims 45-53 be withdrawn and those claims allowed.

b. Lack of motivation to combine references

The Office Action states, with regard to claims 45 and 46:

> [I]t is obvious, and therefore, examiner takes Official Notice that each of the parallel queues 1 through n in Fig. 6, and the output queues (i.e., queues 32, 34, 36, 38, 40, 42, 44, and 46) in Fig 5, can all be located on a shared memory device; for example, Aatresh (USP 6,067,301) discloses a DRAM buffer that holds all output queues, col. 3, lines 25-45; examiner also interprets the pointer-payload memory and queuing structure as one well-known in the art, and, inherently one of many memory structures that can be used in a router, for example, Kadambi et al. (USP 6,707,818) discloses a memory-pointer and memory payload structure for router (EPIC) 20, col. 7, lines 27-44.

Office Action at 19. The Office Action further states, with regard to claim 47:

> Examiner takes Official Notice that it is obvious to implement an algorithm in hardware. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the algorithm in either software or hardware.

Office Action at 20. As shown above in the quoted portions, the Office Action states that 1) it is obvious to employ a shared memory device, 2) it is obvious to implement one of many memory structures that can be used in a router, and 3) it is obvious to implement an algorithm in hardware. The Office Action, however, fails to suggest the desirability for any of the suggested modifications. It is well settled that the fact that references can be combined or modified is not sufficient to establish a *prima facie* case of obviousness, M.P.E.P. § 2143.01. The quoted statements above merely say that the references can be modified, and does not state any desirability for making the modifications. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combinations, M.P.E.P. § 2143.01 citing *In re Mills*, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). Thus, the failure to provide motivation suggesting desirability of the modifications is improper. Accordingly, Applicant respectfully submits that the 35 U.S.C. § 103(a) rejection of claims 45-53 is improper and should be withdrawn.

IV. Conclusion

In view of the above response, Applicant believes the pending application is in condition for allowance.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 06-2380, under Order No. 59182/P007US/10020644 from which the undersigned is authorized to draw.

Dated: March 29, 2005

Respectfully submitted,

By Thomas W. Kelton

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